CLAIMS

1. A method of fabricating a semiconductor device in a semiconductor structure, comprising the steps of:

forming a first, relatively high quality, epitaxial layer on a substrate, the high quality layer including a quantum well;

forming a second, relatively lower quality, epitaxial defect layer on top of the high quality layer; and

thermally processing the structure to effect at least partial diffusion of the defects from the defect layer into the high quality layer in order to achieve quantum well intermixing in the structure.

2. The method of claim 1 in which the high quality epitaxial layer is formed comprising a series of sub-layers.

3. The method of claim 1 in which the defect layer is formed comprising a series of sub-layers.

4. The method of claim 1 further including the step of forming a further high quality epitaxial layer on top of the defect layer prior to the thermal processing step.

5. The method of claim 1 further including the step of forming a cap layer on top of the defect layer.

6. The method of claim 5 in which the cap layer is adapted to inhibit oxidation of the defect layer during subsequent processing.

7. The method of claim 1 in which the defect layer is formed by varying the source element ratio during growth away from ideal or stoichiometric conditions to result in crystalline defects.

8. The method of claim 1 or claim 7 in which the defect layer is formed by varying the substrate temperature away from ideal conditions to result in crystalline defects.

9. The method of claim 7 or claim 8 in which the defect layer comprises a defect density in excess of 1000 defects/cm^2 or 10^6 defects/cm^3.

10. The method of claim 7 or claim 8 in which the defect layer comprises a defect density 10 times higher than that of the high quality layer.

11. The method of claim 10 in which the defect layer comprises a defect density 100 times higher than that of the high quality layer.

12. The method of claim 1 in which the semiconductor device is formed in a III–V crystal structure, including the steps of:

providing a V–III source element ratio during growth of the high quality layer of substantially 1:1; and

providing a V–III source element ratio during growth of the defect layer lying between 1:0.5 and 1:0.05.

13. The method of claim 1 further including the step of photolithographically processing the substrate to spatially define areas of the defect layer over the surface of the substrate.

14. The method of claim 13 in which the defect layer is defined over regions of the structure that will form non-absorbing mirrors of a laser device.

15. The method of claim 1 further including the step of depositing a layer of SiO_2 over the defect layer.

16. The method of claim 1 in which the defect layer is provided having a different thermal expansion coefficient than the high quality layer, the layers being lattice matched such that the difference in thermal expansion creates a localised strain increasing defect production during the thermal processing step.

17. The method of claim 16 in which the defect layer includes at least a AlGaInP layer and the high quality layer includes at least a GaAs layer.

18. The method of claim 16 in which the defect layer includes at least a AlGaAs layer and the high quality layer includes at least a GaAs layer.

19. The method of claim 16 in which the defect layer includes at least a GaInAsP layer and the high quality layer includes at least an InP layer.

20. The method of claim 1 further including the step of incorporating a strain layer within the defect layer to enhance dislocation propagation during the thermal processing step.

21. The method of claim 1 in which the thermal processing step is performed at temperatures of less than 850 degrees C.

22. The method of any preceding claim wherein the semiconductor device formed comprises any one of a laser, a vertical cavity light emitting device, a passive waveguide, an optical integrated circuit or a photonic integrated circuit.

23. A semiconductor device formed in a semiconductor substrate, using the process of any preceding claim, the device including a quantum well intermixed region.

24. A semiconductor device formed substantially as described herein with reference to the accompanying drawings.

25. A method of forming a semiconductor device substantially as described herein with reference to the accompanying drawings.